

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: K. ITOH, et al.

Application No.: Rule 1.53(b) Continuation of U.S. Patent Application Serial No. 10/330,077, filed December 30, 2002

Filed: On Even Date Herewith

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE WITH IMPROVED STORAGE MOSFET ARRANGEMENT (As Amended)

Art Group of Parent: 2818

Examiner of Parent: G. N. Aduong

**INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §1.97 & 1.98**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

March 10, 2004

Sir:

In the matter of the above-identified application, this Information Disclosure Statement is being submitted with the following citation as specified in 37 CFR §1.97(d).

"A copy of any patent, publication or other information listed in an Information Disclosure Statement is not required to be provided if it was previously cited by or submitted to the Office in a prior application, provided that the prior application is properly identified in the statement and relied upon for an earlier filing date under 35 U.S.C. §120."

Applicants are submitting herewith a copy of Form PTO/SB/08A which list documents cited in parent applications Serial No. 10/330,077, filed December 30, 2002, which is a Continuation of application Serial No. 09/959,906, filed November

13, 2001 (now U.S. Patent 6,515,892), the entire disclosure of which is hereby incorporated by reference.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, Deposit Account No. 01-2135 (520.40847CC2).

Respectfully submitted,

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<p>Substitute for form 1449A/PTO</p> <p>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</p> <p>(use as many sheets as necessary)</p>				Complete if Known	
				Application Number	Not assigned yet
				Filing Date	On even date herewith
				First Named Inventor	K. ITOH, et al.
				Art Unit	Not assigned yet
				Examiner Name	Not assigned yet
Sheet	1	of	1	Attorney Docket Number	520.40847CC2

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

OTHER PRIOR ART—NON PATENT LITERATURE DOCUMENTS

EXAMINER'S CITE TO OTHER PRIOR ART - NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Ultra LSI Memories, Baifukan, Nov. 5, 1994, Kiyoo ITOH, pp. 12-15	
		ISSCC '72, VLSI Memory Chip Design, Kiyoo ITOH, pp. 12-13	

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard St.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

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